Freescale Semiconductor
Technical Data

Document Number: MRF9002NR2
Rev. 8, 5/2006

RoHS

RF Power Field Effect Transistor Array

N-Channel Enhancement-Mode Lateral MOSFET

MRF9002NR2

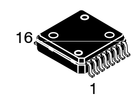
Designed for broadband commercial and industrial applications with frequencies to 1000 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment. The device is in a PFP-16 Power Flat Pack package which gives excellent thermal performances through a solderable backside contact.

- Typical Performance at 960 MHz, 26 Volts
  Output Power — 2 Watts Per Transistor
  Power Gain — 18 dB
  Efficiency — 50%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 960 MHz, 2 Watts CW Output Power

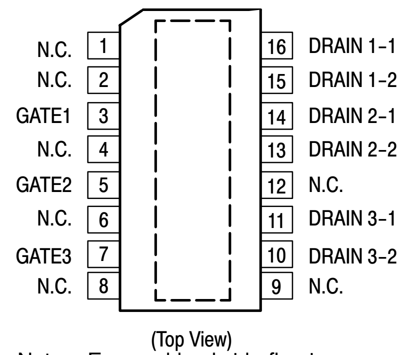
Features

- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- RoHS Compliant
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

1000 MHz, 2 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 978-03
PLASTIC
PFP-16



Note: Exposed backside flag is source terminal for transistors.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Dissipation Per Transistor @ T_C = 25°C	P_D	4	W
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	150	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case, Single Transistor	$R_{\theta JC}$	12	°C/W

Table 3. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

freescale semiconductor

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 20 μAdc)	$V_{GS(th)}$	2.4	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 25 mAdc)	$V_{GS(Q)}$	3	—	5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.1 Adc)	$V_{DS(on)}$	—	0.3	—	Vdc
Functional Tests (Per Transistor in Freescale Test Fixture, 50 ohm system)					
Common-Source Amplifier Power Gain @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	G_{ps}	15	18	—	dB
Drain Efficiency @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	η	35	50	—	%
Input Return Loss @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	IRL	—	-15	-9	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	P_{1dB}	34	37	—	dBm

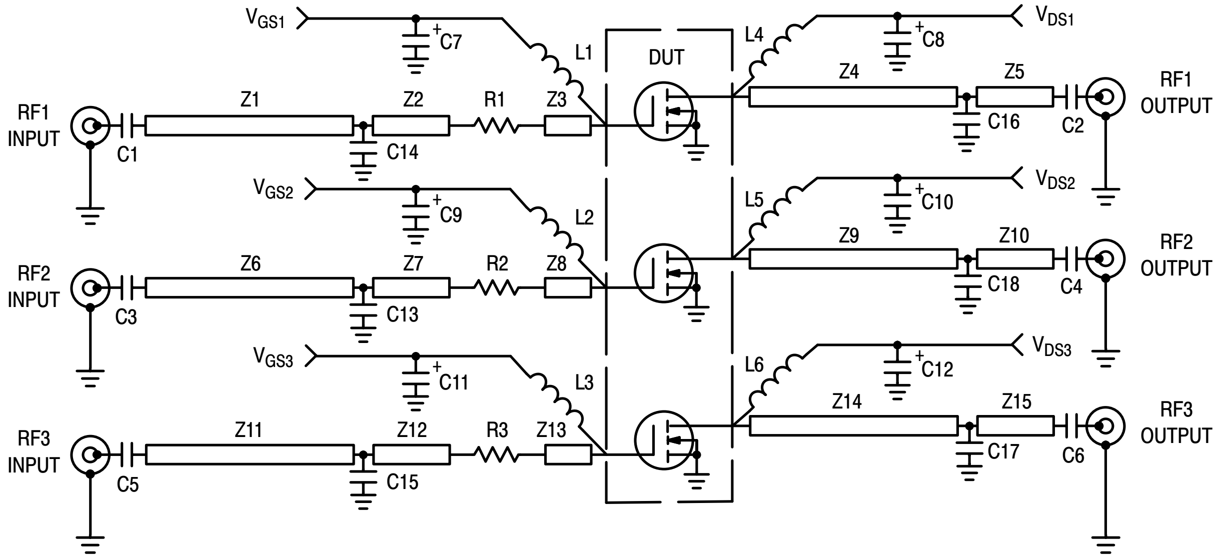
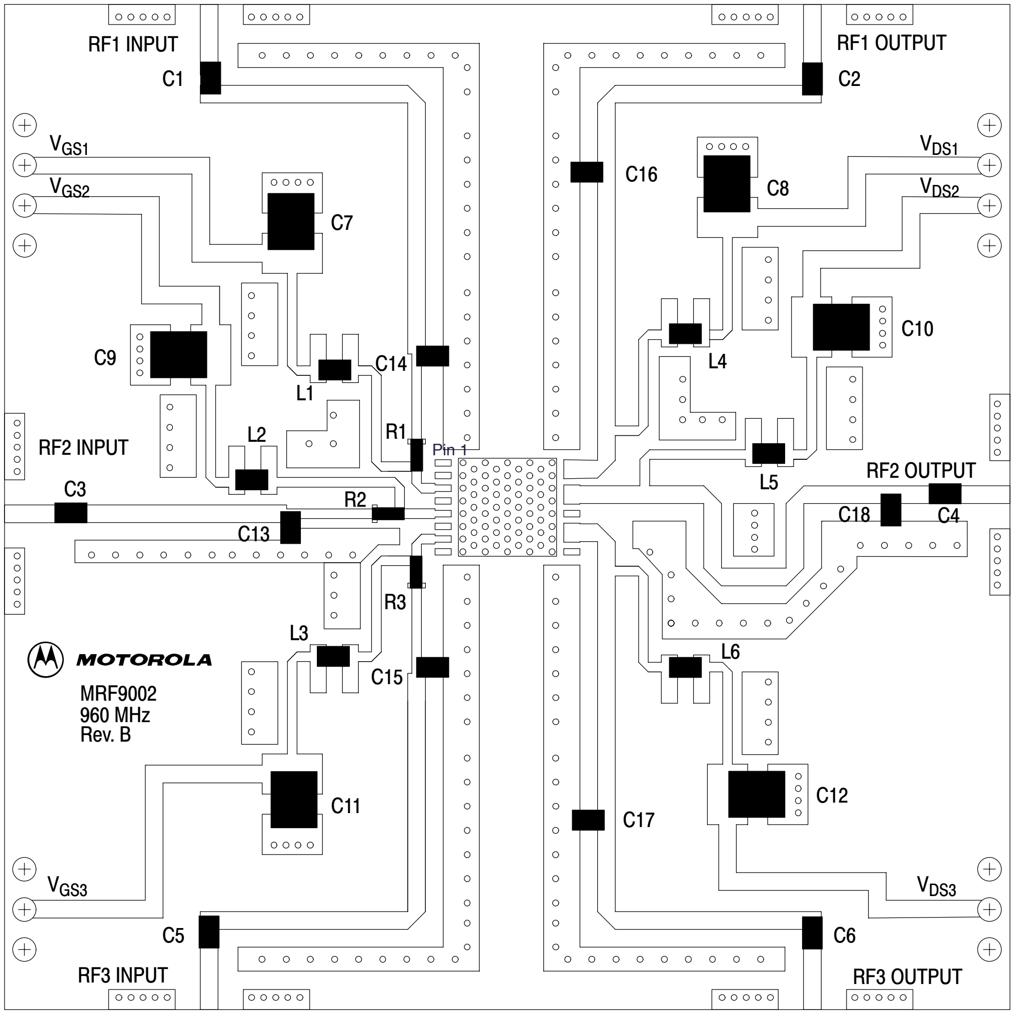


Figure 2. MRF9002NR2 Broadband Test Circuit Schematic

Table 5. MRF9002NR2 Broadband Test Circuit Component Designations and Values

Designators	Description
C1 - C6	33 pF Chip Capacitors (0805)
C7 - C12	1.0 μF, 35 V Tantalum Capacitors, B Case, Kemet
C13	8.2 pF Chip Capacitor (0805)
C14, C15	10 pF Chip Capacitors (0805)
C16, C17	2.7 pF Chip Capacitors (0805)
C18	3.3 pF Chip Capacitor (0805)
L1 - L6	12 nH Chip Inductors (0805)
R1 - R3	0 Ω Chip Resistors (0805)
Z1, Z11	1.16 x 28.5 mm Microstrip
Z2, Z7, Z12	0.65 x 5.6 mm Microstrip
Z3, Z8, Z13	0.65 x 2.6 mm Microstrip
Z4, Z14	1.16 x 19.5 mm Microstrip
Z5, Z15	1.16 x 17.5 mm Microstrip
Z6	1.16 x 12.9 mm Microstrip
Z9	1.16 x 27.2 mm Microstrip
Z10	1.16 x 4.3 mm Microstrip
PCB	Etched Circuit Board
Raw PCB Material	Rogers RO4350, 0.020″, 2.5″, x 2.5″, ε_r = 3.5
Bedstead	Copper Heatsink



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 3. MRF9002NR2 Broadband Test Circuit Component Layout

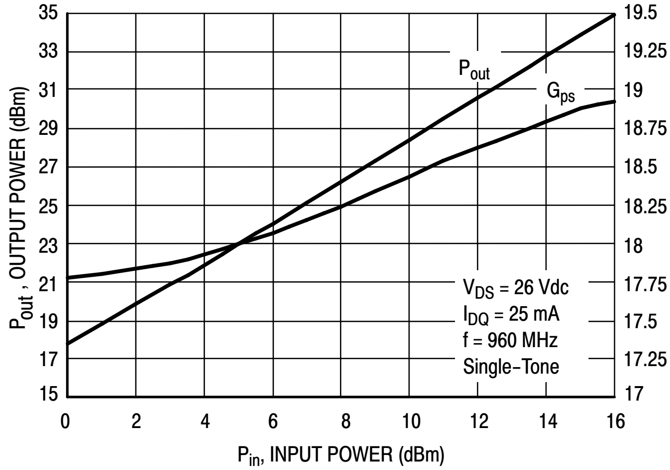


Figure 4. Output Power and Power Gain versus Input Power

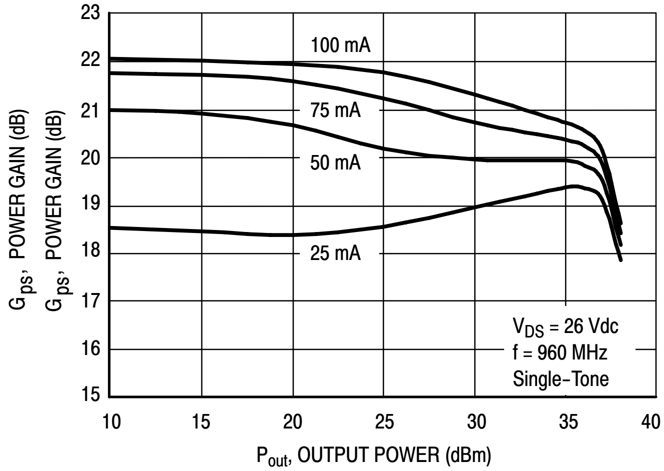


Figure 5. Power Gain versus Output Power

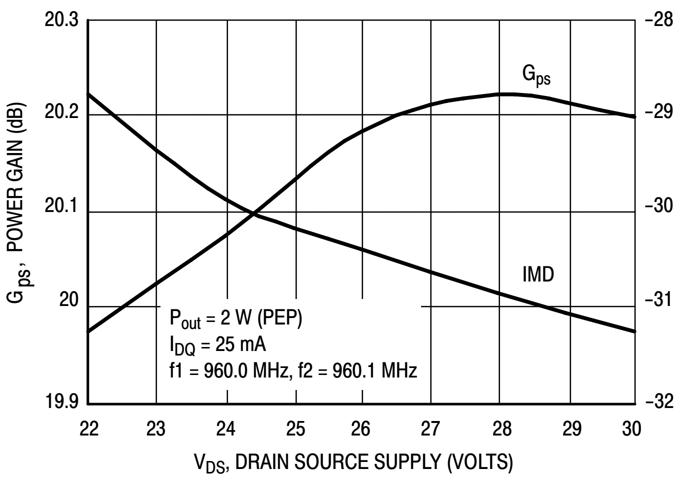


Figure 6. Power Gain and Intermodulation Distortion versus Supply Voltage

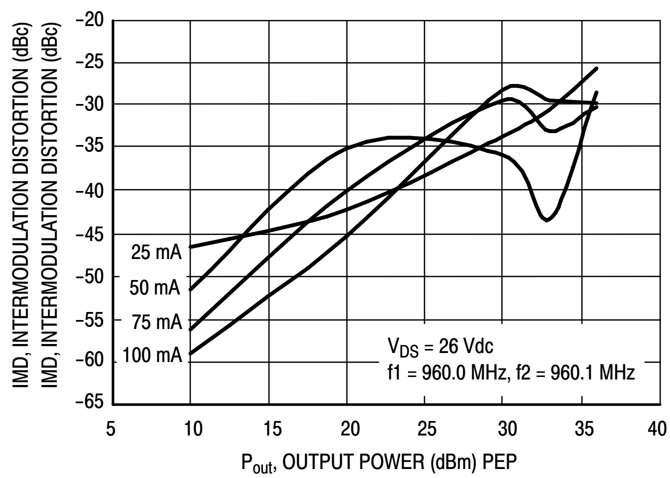


Figure 7. Intermodulation Distortion versus Output Power

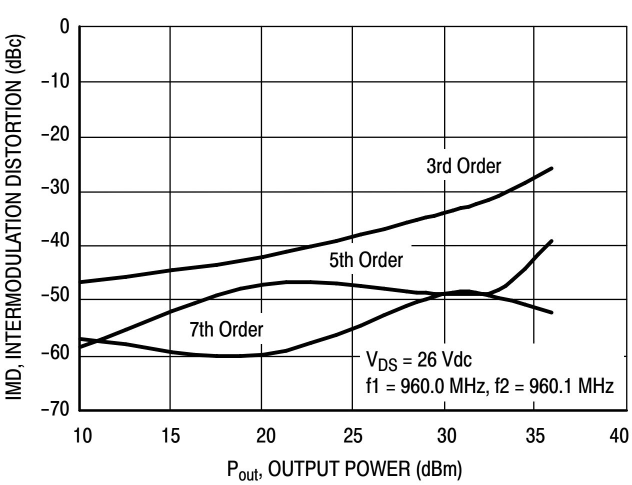


Figure 8. Intermodulation Distortion Products versus Output Power

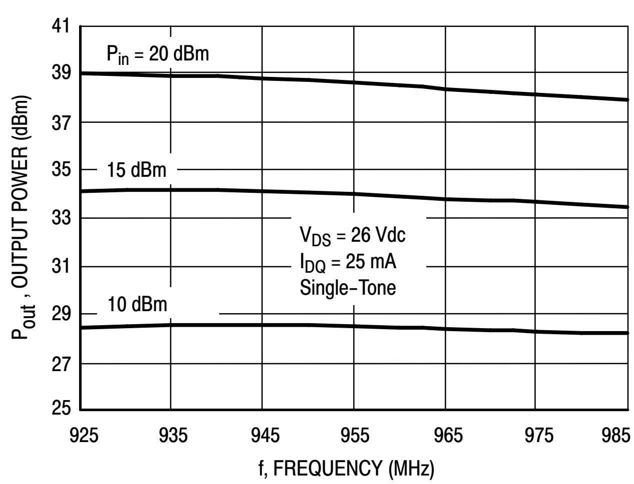


Figure 9. Output Power versus Frequency

TYPICAL CHARACTERISTICS

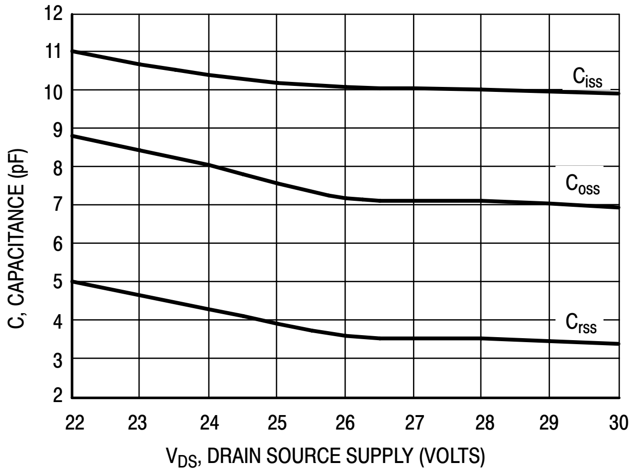
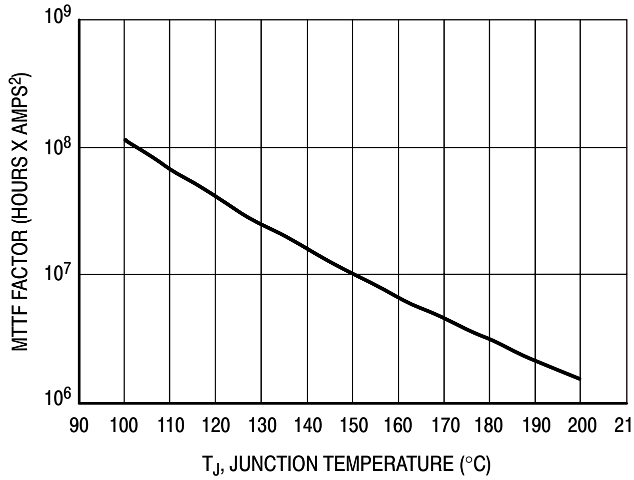
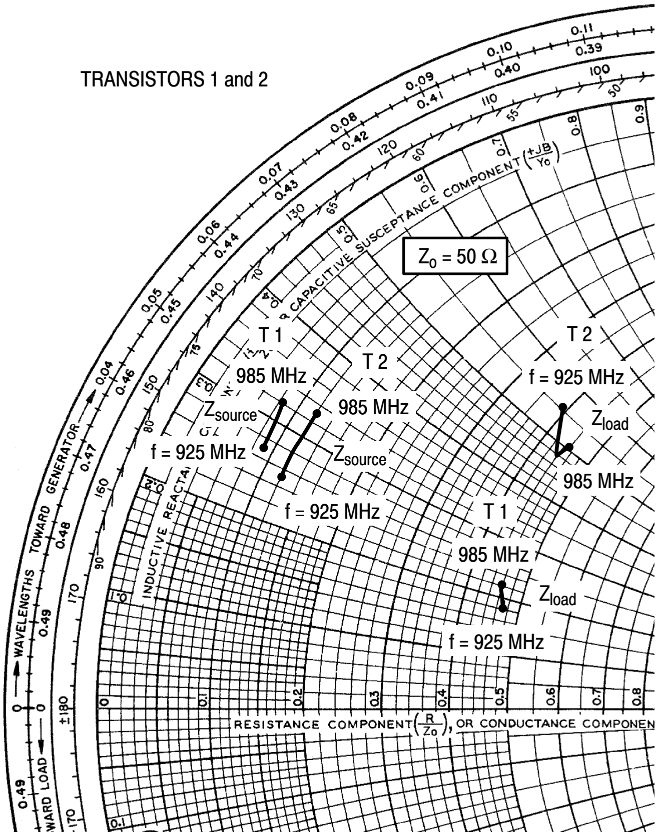


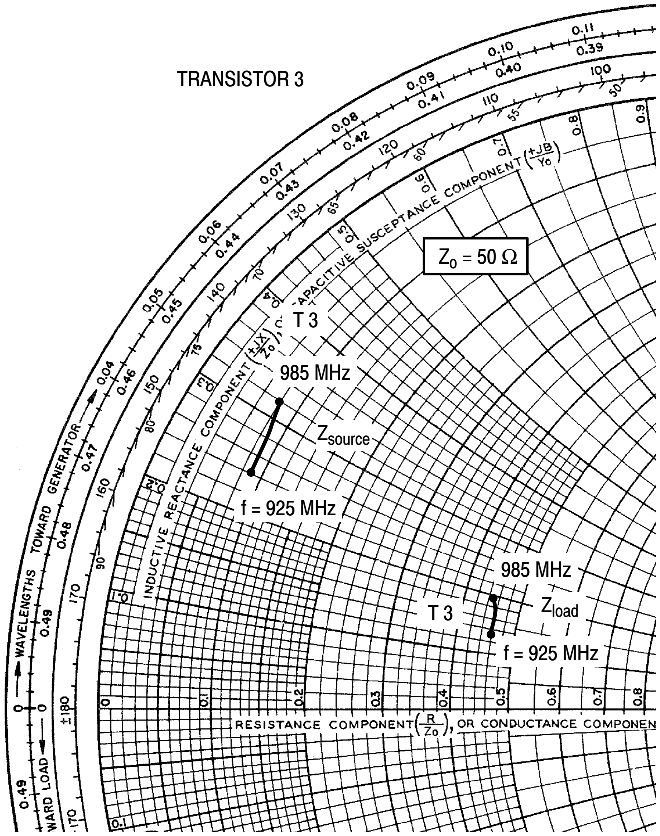
Figure 10. Capacitance versus Drain Source Voltage



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 11. MTTF Factor versus Junction Temperature





V_{DD} = 26 V, I_{DQ} = 25 mA, P_{out} = 2 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
925	4.5 + j13.3	23.4 + j9.2
960	4.3 + j15.3	23.2 + j10.4
985	4.1 + j15.8	23.0 + j11.1

Transistor 1

V_{DD} = 26 V, I_{DQ} = 25 mA, P_{out} = 2 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
925	6.0 + j12.3	19.7 + j27.8
960	5.9 + j14.3	22.0 + j23.9
985	5.8 + j16.5	22.5 + j25.4

Transistor 2

V_{DD} = 26 V, I_{DQ} = 25 mA, P_{out} = 2 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
925	4.3 + j12.2	23.1 + j6.5
960	4.3 + j14.0	22.8 + j8.4
985	3.9 + j15.9	22.6 + j9.3

Transistor 3

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

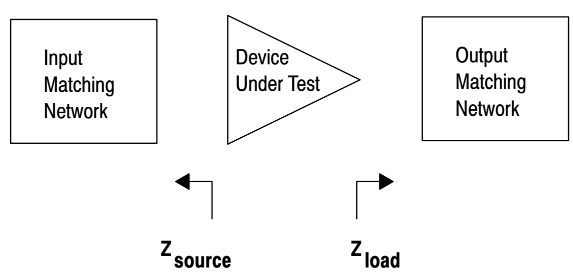


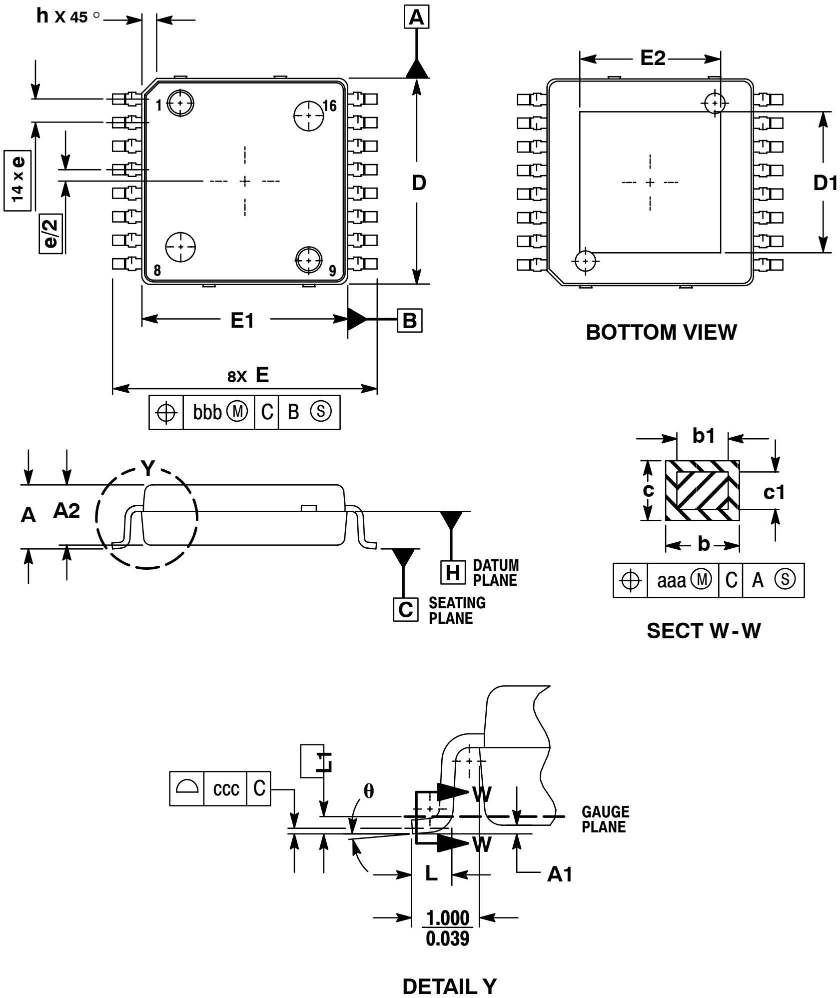
Figure 12. Series Equivalent Source and Load Impedance

NOTES

NOTES

NOTES

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978-03
ISSUE C
PLASTIC
PFP-16

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

freescale™ semiconductor

Document Number: MRF9002NR2
Rev. 8, 5/2006